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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,708	08/28/2001	Sreekrishnan Venkiteswaran	JP920010119US1	5774

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	7

DATE MAILED: 04/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/940,708	VENKITESWARAN, SREEKRISHNAN
	Examiner	Art Unit
	Woo H. Choi	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-19* is/are allowed.

6)☒ Claim(s) *1-6 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 20 is incomprehensible. It is not clear what is being claimed. Claim 21 depends from claim 20.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 3, 23 – 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Colley *et al.* (US Patent No. 5,577,224, hereinafter "Colley").

With respect to claims 1 and 23 – 27, Colley discloses a method of maintaining the memory contents of a memory medium having a plurality of memory sectors that are erased before being rewritten (this limitation is not give any weight since it is not 'necessary to give life, meaning, and vitality' to the claims, see MPEP 2001.02), the method comprising the steps of:

maintaining a plurality of independent sector caches each respectively corresponding with a stored memory sector of the memory medium (col. 63, 43 – 53);

writing data to one or more of said sector caches with required changes to the corresponding stored memory sectors of the memory medium (col. 63, lines 55 – 65, buffer descriptor fields cacmod and modified); and

accessing the contents of said stored memory sectors from the corresponding sector caches, if said contents are stored in said corresponding sector caches.

5. With respect to claim 2, the sector caches are recorded as a linked list memory structure of said cached memory sectors (col. 64, 48 – 50).

6. With respect to claim 3, the linked list comprises a finite number of said independent sector caches (this is inherent in any caching system since the amount of memory available for caching in a practical system is finite).

7. Claims 1 – 6, 20 – 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogawa *et al.* (US Patent No. 5,933,847, hereinafter "Ogawa").

8 With respect to claims 1, 23 – 27, Ogawa discloses a method of maintaining the memory contents of a memory medium having a plurality of memory sectors that are erased before being rewritten, the method comprising the steps of:

maintaining a plurality of independent sector caches each respectively corresponding with a stored memory sector of the memory medium (figure 12);

writing data to one or more of said sector caches with required changes to the corresponding stored memory sectors of the memory medium (figure 14); and

accessing the contents of said stored memory sectors from the corresponding sector caches, if said contents are stored in said corresponding sector caches (figure 13).

9. With respect to claim 2, the sector caches are recorded as a linked list memory structure of said cached memory sectors (figure 12).

10. With respect to claim 3, the linked list comprises a finite number of said independent sector caches (figure 12).

11. With respect to claim 4, the contents of each of the stored memory sectors of the memory medium comprises a number of blocks (figure 12, one block).

12. With respect to claim 5, the method further includes the step of:

maintaining a record, for each of the sector caches, of the number of dirty blocks for which the contents of a sector cache and the corresponding stored memory sector are not currently equivalent (figure 12, change or dirty state of each block is recorded).

13. With respect to claim 6, the method further comprises the step of:

incrementing the recorded number of dirty blocks for a sector cache after performing said step of writing data to the corresponding sector cache in respect of said stored memory sector, if the block for which said step of writing data is performed is not currently marked as dirty (figure 8, step S42, change state of the block is marked YES which is equivalent to incrementing the number of dirty blocks from 0 to 1).

14. With respect to claim 20, since the original claim is incomprehensible, for the purposes of this examination the claim will be interpreted as follows: one or more reserved sector caches persistently store sectors that correspond to stored memory sectors of the memory medium (the cache is reserved for FAT, the cache persistently stores FAT information).

15. With respect to claims 21, the reserved sector caches correspond with stored memory sectors in respect of which the step of writing data to the cached memory sectors frequently occurs (FAT information changes every time there's a change in any of the files, therefore, the FAT sector changes much more frequently that other sectors).

16. With respect to claim 22, the reserved sector caches correspond with stored memory sectors for which critical system meta-data is stored (FAT contains meta-data).

17. Claims 1 – 6, and 23 – 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (US Patent Application Publication 2002/0166022).

18. With respect to claims 1, 23 – 27, Suzuki discloses a method of maintaining the memory contents of a memory medium having a plurality of memory sectors that are erased before being rewritten, the method comprising the steps of:

maintaining a plurality of independent sector caches each respectively corresponding with a stored memory sector of the memory medium (figure 6);

writing data to one or more of said sector caches with required changes to the corresponding stored memory sectors of the memory medium (figure 7); and

accessing the contents of said stored memory sectors from the corresponding sector caches, if said contents are stored in said corresponding sector caches (figure 6).

19. With respect to claim 2, the sector caches are recorded as a linked list memory structure of said cached memory sectors (figure 6).

20. With respect to claim 3, the linked list comprises a finite number of said independent sector caches (figure 6).

21. With respect to claim 4, the contents of each of the stored memory sectors of the memory medium comprises a number of blocks (figure 6, one block).

22. With respect to claim 5, the method further includes the step of:

maintaining a record, for each of the sector caches, of the number of dirty blocks for which the contents of a sector cache and the corresponding stored memory sector are not currently equivalent (figure 6, dirty state of each block is recorded).

23. With respect to claim 6, the method further comprises the step of:

incrementing the recorded number of dirty blocks for a sector cache after performing said step of writing data to the corresponding sector cache in respect of said stored memory sector, if the block for which said step of writing data is performed is not currently marked as dirty (figure 8, step S42, dirty state of the block is marked YES which is equivalent to incrementing the number of dirty blocks from 0 to 1).

Allowable Subject Matter

24. Claims 7 – 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bruce et al. (US Patent No. 6,000,006 and US Patent Application Publication

2002/0097594) disclose flash memory systems with cache. Howard et al. (US Patent Application Publication No. 2002/0073276) discloses a memory system with cache and dirty block indications. DeWitt et al (US Patent No. 5,577,224), Haines et al. (US Patent Publication No. 2002/0091895) and Otterness et al. (US Patent No. 6,460,122) disclose other memory systems with caches that are organized with as linked lists.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc/MK
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April 1, 2004

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